This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-10 (Cancelled)

B1

11. (Currently Amended) An interconnect structure for a semiconductor chip comprising:

a nonreflowed solder assembly including;

a Pb-rich ball attached to said semiconductor chip and having an exposed surface; and

a thin layer of Sn ~~deposited~~ on said exposed surface of said Pb-rich ball;

~~wherein~~ said Sn layer being sufficiently thin and having a melting temperature lower than that of Pb so that Sn from said thin layer and Pb from said ball are diffused and intermixed after reflowing and annealing to form an assembly having a weight composition of about 97/3 Pb/Sn.

12. (Original) The interconnect structure of claim 11, wherein said thin layer of Sn has a thickness of less than 10.2 μm (0.4 mils).

13. (Currently Amended) An interconnect structure comprising a substrate, said substrate having a nonreflowed solder assembly having at least one Pb-rich ball and at least a portion of said Pb-rich ball having thereon at least one thin coating of a low melting point metal, ~~wherein~~ the melting point of said low melting point metal is lower than the melting point of said Pb-rich ball, and the low melting point metal is sufficiently thin so that after reflowing and annealing said low melting point metal and Pb from said ball are diffused and intermixed to form an assembly having a relatively high melting point.

14. (Original) The interconnect structure of claim 13, wherein the thin coating of the low melting point metal has a thickness of less than 10.2 μm (0.4 mils).

15-19 (Withdrawn)